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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,812	12/08/2003	Yu Chang Kim	40296-0041	9240

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EXAMINER	
GURLEY, LYNNE ANN	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,812	KIM ET AL.	
	Examiner	Art Unit	
	Lynne A. Gurley	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because lines 1-3 appear to be a direct translation to English (i.e. "manufacturing metal line of semiconductor device" should be "manufacturing a metal line of a semiconductor device"). Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities:

3. On page 1, line 6, "method" should be "a method".

4. On page 1, line 7, "metal line or semiconductor device" should be " a metal line of a semiconductor device".

5. On page 1, line 22, "an upper and a lower wiring layers" should be "upper and lower wiring layers" or "an upper and a lower wiring layer".

6. On page 3, lines 5-6, "first insulating film 13" should be "first etch barrier film 15" (See drawing fig. 1a).

7. On page 8, line 24, "first insulating film 45" should be "first insulating film 45" (see figs. 3a).

8. On page 8, line 25 to page 9, line 1, the same error occurs.

9. On page 9, line 5, the same error occurs.

10. On page 10, line 13, "anti-reflection film 52" should be "anti-reflection film 53" (see fig. 3e).

Appropriate correction is required.

11. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification, especially areas where the language and sentence structure appears to be the result of direct translation.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 11 and, lines13-14, the following limitation: "first interlayer insulating film" is indefinite in that it is the "first etch barrier film", which is exposed and then removed, instead of the "first interlayer insulating film". Therefore, the limitation "interlayer insulating", in both instances, should be replaced with the limitation "etch barrier".

Additionally, "a" should be inserted in line 1 of claim 1 after "metal lines of".

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Harada et al. (US 6,251,774, dated 6/26/01).

16. Harada shows the method as claimed in figures 1-14 and corresponding text, with emphasis on figures 4A-4G, as: forming a first interlayer insulating film exposing a top portion of a lower metal line on a semiconductor substrate (metal 30 in insulator on substrate; column 5, lines 15-21; column 8, lines 15-67; column 9, lines 1-67; column 10, lines 1-54); forming a stacked structure of a first etch barrier 32, a second interlayer insulating film 34, a second etch barrier film 36, a third interlayer insulating film 38 and an anti-reflection film 58 (column 9, lines 40-50); etching the stacked structure to form a via contact hole 46 exposing a portion of the first etch barrier film on the lower metal line (fig. 4C); removing the exposed portion of the first etch barrier film to expose the lower metal line (column 9, lines 44-47; fig. 4G to the step in fig. 1F); forming a photoresist film 48 on the entire surface; subjecting the photoresist film to an exposure and development process using an upper metal line mask to form a photoresist film pattern for defining an upper metal line region, wherein the photoresist film pattern further fills a portion of the via contact hole (figs. 4D-4E); etching the anti-reflection film and the third interlayer insulating film using the photoresist film pattern as a mask to form the upper metal line region (fig. 4F); removing the photoresist pattern (fig. 4F) and forming an upper metal line contacting the lower metal line by filling the upper metal line region (column 9, lines 44-47). The first and second etch barrier films are SiN films. The second and third interlayer insulating films are low-k silica-base films, oxide films (column 8, lines 30-49).

17. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagahara (US 2002/0192945, dated 12/19/02, filed 6/11/02).

18. Nagahara shows the method as claimed in figures 1-10 and corresponding text, as: forming a first interlayer insulating film exposing a top portion of a lower metal line on a semiconductor substrate (metal 8 in insulator on substrate; [0079]); forming a stacked structure of a first etch barrier 7, a second interlayer insulating film 6, a second etch barrier film 5, a third interlayer insulating film 4/with cap layer 3 and an anti-reflection film (BARC not shown [0080]); etching the stacked structure to form a via contact hole 46 exposing a portion of the first etch barrier film on the lower metal line (fig. 1B); removing the exposed portion of the first etch barrier film to expose the lower metal line (fig. 3B); forming a photoresist film 1 (fig. 2A) on the entire surface; subjecting the photoresist film to an exposure and development process using an upper metal line mask to form a photoresist film pattern for defining an upper metal line region, wherein the photoresist film pattern further fills a portion of the via contact hole (fig. 2B); etching the anti-reflection film and the third interlayer insulating film using the photoresist film pattern as a mask to form the upper metal line region (fig. 2C-3A); removing the photoresist pattern (fig. 3B) and forming an upper metal line contacting the lower metal line by filling the upper metal line region (fig. 3C). The first and second etch barrier films are SiC or SiN films. The second and third interlayer insulating films are low-k silica-base films, oxide films [0115].

19. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (US 6,642,153, dated 11/4/03).

20. Chang shows the method as claimed in figures 2A-2F and corresponding text, as: forming a first interlayer insulating film exposing a top portion of a lower metal line on a semiconductor substrate (metal 20 in insulator on substrate); forming a stacked structure of a first etch barrier 22A, a second interlayer insulating film 24A, a second etch barrier film 22B, a third interlayer insulating film 24B and an anti-reflection film 26 (SiON BARC); etching the stacked structure to form a via contact hole 28A exposing a portion of the first etch barrier film on the lower metal line (fig. 2B); removing the exposed portion of the first etch barrier film to expose the lower metal line (fig. 2F); forming a photoresist film 30 on the entire surface; subjecting the photoresist film to an exposure and development process using an upper metal line mask to form a photoresist film pattern for defining an upper metal line region, wherein the photoresist film pattern further fills a portion of the via contact hole (fig. 2D); etching the anti-reflection film and the third interlayer insulating film using the photoresist film pattern as a mask to form the upper metal line region (fig. 2E); removing the photoresist pattern (figs. 2E-2F; column 5, lines 35-67; column 6, lines 1-48) and forming an upper metal line contacting the lower metal line by filling the upper metal line region (column 6, lines 49-67). Fluorocarbons and oxygen are discussed as etchants for the dielectric layers (column 5, lines 1-10). The first and second etch barrier films are SiN or SiC films. The second and third interlayer insulating films are low-k silica-base films, oxide films (column 4, lines 27-67).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

23. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

24. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 6,251,774, dated 6/26/01) in view of Chang et al. (US 6,642,153, dated 11/4/03, filed 7/31/02) and further in view of Wang et al. (US 6,521,524, dated 2/18/03, filed 2/7/01).

Harada shows the method substantially as claimed and as described in the previous paragraphs.

Harada lacks anticipation only in not teaching that the anti-reflection film is SiON organic; the anti-reflection film and the third interlayer insulating film are etched with plasma using CF4/O2/Ar; and, the removal step for the photoresist in the via contact is performed in-situ.

Chang teaches, in a similar method, where a photoresist plug is used to protect underlying layers during patterning and two etch stops in between insulating layers are used to pattern a dual damascene structure, the use of SiON for an anti-reflecting film 26. The same materials are taught for the structure layers.

Wang teaches the plasma etch with CF4/O2/Ar for the same dielectric layers (column 6, lines 1-10; column 5, lines 30-42).

It would have been obvious to one of ordinary skill in the art to have had the anti-reflection film be SiON; to have had the anti-reflection film and the third interlayer insulating film be etched with plasma using CF4/O2/Ar; and, to have had the removal step for the photoresist in the via contact be performed in-situ, in the method of Harada, with the motivation being given by Chang, that SiON is conventional as an anti-reflection layer in a similar process with the same materials; with the motivation being given by Wang, that plasma etch with CF4/O2/Ar etches the same insulating layers; and, with the motivation that an in-situ removal step is conventional, prevents intermediate contamination of the insulation layers and, improves the efficiency of the steps in the method.

25. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagahara et al. (US 2002/0192945, dated 12/19/02, filed 6/11/02) in view of Chang et al. (US 6,642,153,

dated 11/4/03, filed 7/31/02) and further in view of Wang et al. (US 6,521,524, dated 2/18/03, filed 2/7/01).

Nagahara shows the method substantially as claimed and as described in the previous paragraphs.

Nagahara lacks anticipation only in not teaching that the anti-reflection film is SiON organic; the anti-reflection film and the third interlayer insulating film are etched with plasma using CF4/O2/Ar; and, the removal step for the photoresist in the via contact is performed in-situ.

Chang teaches, in a similar method, where a photoresist plug is used to protect underlying layers during patterning and two etch stops in between insulating layers are used to pattern a dual damascene structure, the use of SiON for an anti-reflecting film 26. The same materials are taught for the structure layers.

Wang teaches the plasma etch with CF4/O2/Ar for the same dielectric layers (column 6, lines 1-10; column 5, lines 30-42).

It would have been obvious to one of ordinary skill in the art to have had the anti-reflection film be SiON; to have had the anti-reflection film and the third interlayer insulating film be etched with plasma using CF4/O2/Ar; and, to have had the removal step for the photoresist in the via contact be performed in-situ, in the method of Nagahara, with the motivation being given by Chang, that SiON is conventional as an anti-reflection layer in a similar process with the same materials; with the motivation being given by Wang, that plasma etch with CF4/O2/Ar etches the same insulating layers; and, with the motivation that an in-situ

removal step is conventional, prevents intermediate contamination of the insulation layers and, improves the efficiency of the steps in the method.

26. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 6,642,153, dated 11/4/03, filed 7/31/02) in view of Wang et al. (US 6,521,524, dated 2/18/03, filed 2/7/01).

Chang shows the method substantially as claimed and as described in the previous paragraphs.

Chang lacks anticipation only in not teaching that the anti-reflection film and the third interlayer insulating film are etched with plasma using CF4/O2/Ar; and, the removal step for the photoresist in the via contact is performed in-situ.

Wang teaches the plasma etch with CF4/O2/Ar for the same dielectric layers (column 6, lines 1-10; column 5, lines 30-42).

It would have been obvious to one of ordinary skill in the to have had the anti-reflection film and the third interlayer insulating film be etched with plasma using CF4/O2/Ar; and, to have had the removal step for the photoresist in the via contact be performed in-situ, in the method of Chang, with the motivation being given by Wang, that plasma etch with CF4/O2/Ar etches the same insulating layers; and, with the motivation that an in-situ removal step is conventional, prevents intermediate contamination of the insulation layers and, improves the efficiency of the steps in the method.

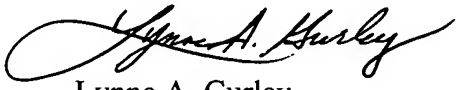
Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the PTO Form 892 for very relevant prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lynne A. Gurley
Primary Patent Examiner
TC 2800, Art Unit 2812

LAG
July 23, 2004